What is claimed is:

1. An on-chip temperature detection device, comprising:

a bipolar type power transistor;

a mirror transistor in which a collector current, which is proportional to a collector current of said power transistor, flows;

a current detection section that detects the collector current of said mirror transistor;

a voltage detection section that detects a voltage between a base and an emitter of said power transistor; and

a calculation section that calculates a chip temperature of said power transistor, based upon the collector current of said mirror transistor detected by said current detection section, and upon the voltage between the base and the emitter of said power transistor detected by said voltage detection section.

2. An on-chip temperature detection device according to Claim 1, wherein:

a collector terminal of said power transistor and a collector terminal of said mirror transistor are connected together, and a base terminal of said power transistor and a base terminal of said mirror transistor are connected together; and

an emitter terminal of said power transistor and an emitter terminal of said mirror transistor are provided independently.

3. An on-chip temperature detection device according to Claim 1, wherein:

said power transistor is driven by a first drive signal;

a second drive signal generation circuit that generates a second drive signal which is a different signal from said first drive signal, and which drives said power transistor so that the voltage between the base and the emitter of said power transistor is less than a predetermined voltage, is further provided; and

said calculation section calculates the chip temperature of said power transistor, based upon the collector current of said mirror transistor detected by said current detection section and upon the voltage between the base and the emitter of said power transistor detected by said voltage detection section, when said power transistor is being driven by said second drive signal.

4. An on-chip temperature detection device according to Claim 3, wherein

said second drive signal generation circuit generates said second drive signal so as to make an electrical potential

of an emitter of said mirror transistor substantially equal to an electrical potential of the emitter of said power transistor.

5. An on-chip temperature detection device according to Claim 3, wherein

said second drive signal generation circuit outputs said second drive signal for a predetermined period when said first drive signal is OFF.

6. An on-chip temperature detection device, comprising:

a bipolar type power transistor that is driven by a first drive signal;

a voltage detection section that detects a voltage between a base and an emitter of said power transistor;

a second drive signal generation circuit that generates a second drive signal which is a different signal from said first drive signal, and which drives said power transistor so that the voltage between the base and the emitter of said power transistor is less than a predetermined voltage; and

a calculation section which calculates a chip temperature of said power transistor, when said power transistor is being driven by said second drive signal, based upon at least the voltage between the base and the emitter of said power transistor detected by said voltage detection

section.

7. An on-chip temperature detection device according to Claim 6, wherein

said second drive signal generation circuit outputs said second drive signal for a predetermined period when said first drive signal is OFF.

8. An on-chip temperature detection device, comprising:

a bipolar type power transistor that is driven by a first drive signal;

a mirror transistor in which a collector current, which is proportional to a collector current of said power transistor, flows, when said power transistor is being driven by said first drive signal;

a second drive signal generation circuit that generates a second drive signal which is a different signal from said first drive signal, which causes a predetermined current to flow in said mirror transistor so that a voltage between a base and an emitter of said mirror transistor is less than a predetermined voltage, and which drives said power transistor to be OFF;

a voltage detection section that detects the voltage between the base and the emitter of said mirror transistor; and

a calculation section that calculates a chip temperature of said power transistor, when said mirror transistor and said power transistor are being driven by said second drive signal, based upon at least the voltage between the base and the emitter of said mirror transistor detected by said voltage detection section.

9. An on-chip temperature detection device according to Claim 8, wherein

said second drive signal generation circuit outputs said second drive signal for a predetermined period when said first drive signal is OFF.

10. An on-chip temperature detection device, comprising:

a bipolar type power transistor that is driven by a first drive signal;

a mirror transistor in which a collector current, which is proportional to the collector current of said power transistor, flows, when said power transistor is being driven by said first drive signal;

an OFF signal generation circuit that generates an OFF signal which turns said power transistor OFF when said first drive signal is OFF;

a current drive circuit that flows a predetermined current in said mirror transistor so that a voltage between

a base and an emitter of said mirror transistor is less than a predetermined voltage, when said first drive signal is OFF and said power transistor is turned OFF by said OFF signal;

a voltage detection section that detects the voltage between the base and the emitter of said mirror transistor; and

a calculation section that calculates a chip temperature of said power transistor, when said first drive signal is OFF and said power transistor is turned OFF by said OFF signal, based upon at least the voltage between said base and said emitter of said mirror transistor detected by said voltage detection section.

11. An on-chip temperature detection device according to Claim 10, wherein

said OFF signal generation circuit outputs said OFF signal for turning said power transistor OFF for a predetermined period when said first drive signal is OFF.

12. An on-chip temperature detection device according to Claim 10, wherein:

said current drive circuit comprises a first current drive circuit which flows a first predetermined current in said mirror transistor and a second current drive circuit which flows a second predetermined current in said mirror

transistor, so that the voltage between the base and the emitter of said mirror transistor is less than a predetermined voltage, when said first drive signal is OFF and said power transistor is turned OFF by said OFF signal;

said voltage detection section detects a first voltage between the base and the emitter of said mirror transistor when said first predetermined current is flowing in said mirror transistor, and a second voltage between the base and the emitter of said mirror transistor when said second predetermined current is flowing in said mirror transistor; and

said calculation section calculates the chip temperature of said power transistor, based upon at least said first and said second voltages between the base and the emitter of said mirror transistor detected by said voltage detection section.

13. An on-chip temperature detection device, comprising:

a power transistor that may be a bipolar type or a MOS type including an IGBT, having a collector or drain terminal, an emitter or source terminal, and a base or gate terminal;

a mirror transistor having a collector or drain terminal and a base or gate terminal which are the same, respectively, as said collector or drain terminal and said base or gate terminal of said power transistor, and a mirror

emitter or mirror source terminal which is independent from said emitter or source terminal of said power transistor;

a control circuit that keeps a collector or drain current which flows in said mirror transistor constant; and

a calculation section that flows a predetermined current in a collector or drain of said mirror transistor only while said power transistor is OFF, that measures the voltage between said base or gate terminal and said emitter or source terminal of said mirror transistor at this time, and that calculates the chip temperature of said power transistor based on a temperature characteristic of said voltage.

14. An on-chip temperature detection device according to Claim 13, wherein

said control circuit performs control so as to keep the collector or drain current which flows in said mirror transistor constant, by controlling an electrical potential of said base or gate terminal so that an electrical potential of said mirror emitter or mirror source terminal of said mirror transistor is kept substantially equal to an electrical potential of said emitter or source terminal of said power transistor.

15. An on-chip temperature detection device according to Claim 13, wherein

said control circuit performs control so as to keep a collector or drain current which flows in said mirror transistor constant, and moreover so that no current flows in said power transistor, by controlling an electrical potential of said mirror emitter or mirror source terminal so that an electrical potential of said base or gate terminal is kept equal to or smaller than an electrical potential of said emitter or source terminal of said power transistor.

16. An on-chip temperature detection device according to Claim 13, wherein

said control circuit controls the predetermined current in the collector or drain of said mirror transistor so as to flow in pulse form for a constant short time period while said power transistor is OFF.

17. An on-chip temperature detection device, comprising:

a power transistor that supplies a current based upon a drive signal;

a mirror transistor in which flows a current which is proportional to said current being supplied by and flowing in said power transistor;

a current detection means for detecting said current flowing in said mirror transistor;

a voltage detection means for detecting a voltage

between a drive signal input terminal and a current supply terminal of said power transistor; and

a calculation means for calculating a chip temperature of said power transistor, based upon at least one of said current detected by said current detection means and said voltage detected by said voltage detection means.